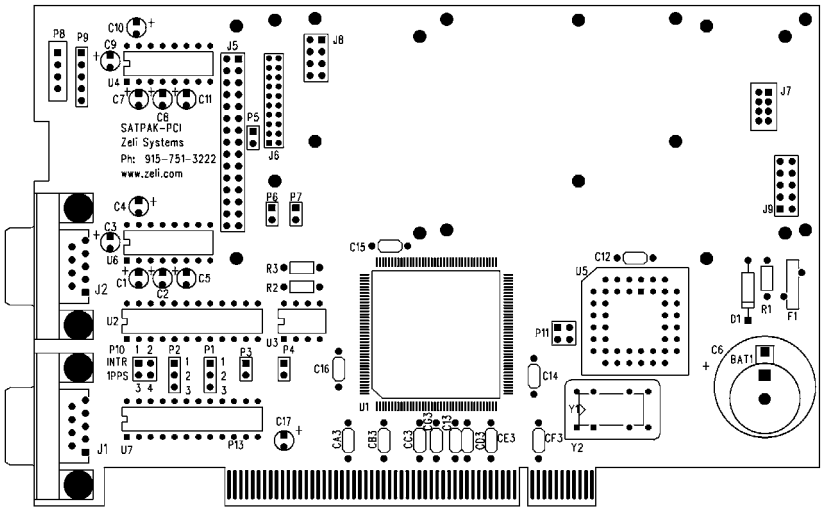
Zeli Systems
SATPAK-PCI



The "*No Hassle*" GPS solution for the PCI Bus

Features:

- The SATPAK-PCI is a carrier board that provides modular GPS receiver technology to the PCI Bus.
- The SATPAK-PCI can be configured to mate with the Trimble ACEII/ACEIII, Trimble SK2/SK8 (Lassen), Navman Jupiter, Canadian Marconi SuperstarII, Motorola M12/VP/GT/UT Oncore, Ashtech G12, or Thales DG14/DG16 GPS receiver.
- Fused +5V to GPS receiver.
- Employs a PLX 9050 PCI Bus Target Interface Chip to communicate with PC16550 Universal Asynchronous Receiver Transmitter (UART) interface to GPS receiver.
- UART and PCI Bus can be bypassed to provide RS-232 signal levels at front panel for both communication channels of GPS receiver via DB9S connectors J2 and J3.
- PCI bus interrupts can be selected from the 1 pulse per second (1PPS) generated by GPS receiver or the interrupt signal associated with UART (see block diagram over).
- Uses a 1 Farad capacitor to retain almanac, ephemeris, and real-time clock of the selected GPS receiver.
- Time Pulse output (1PPS) provided on bracket mount DB9S connectors J2 and J3.
- 1PPS interrupt to the PCI Bus for NTP or timing applications.

SATPAK-PCI Function: The SATPAK-PCI provides an inexpensive method to interface a modular GPS receiver to the PCI Bus. The GPS receiver attaches to the SATPAK-PCI as a daughter-board and GPS antenna input is attached to the BNC (SMA optional) connector located on the SATPAK-PCI bracket. The SATPAK-PCI can be configured to mate with the Trimble ACEII/ACEIII, Trimble SK2/SK8 (Lassen), Navman Jupiter, Canadian Marconi SuperstarII, Motorola M12/VP/GT/UT Oncore, Ashtech G12, or Thales DG14/DG16 GPS receiver. The TTL communication signals of the selected GPS receiver are transmitted and received over the PCI Bus using a PLX 9050 Bus Target Interface Chip and universal asynchronous receiver transmitter (UART). For users that employ external serial ports, the UART can be bypassed to provide RS232 signal levels to two (one for each GPS I/O channel) DB9S connectors on the front panel. A keep-alive voltage is generated by using a large value (1 Farad) capacitor to maintain the almanac, ephemeris, and real-time clock of the selected receiver. Differential GPS (DGPS) corrections can be received at the J3 front panel DB9S connector. Each DB9S connector also provides the 1PPS timing pulse generated by the GPS receiver. A 1PPS interrupt capability allows the SATPAK-PCI to generate a PCI Bus interrupt from the Time Pulse (1PPS) signal generated by the GPS receiver.

Power: The SATPAK-PCI operates from single +5 VDC power. The GPS receiver +5 volt power is fused using a resetable fuse that is thermally activated. Once the fault condition has been removed, the fuse will automatically reset after cooling.

GPS Receiver Communication: The SATPAK-PCI can communicate with the on-board GPS receiver using one of two selectable methods. The typical method is to communicate with the primary GPS I/O channel via the PCI Bus interface. The alternate method is to bypass the PCI interface and communicate with the primary GPS I/O channel using the DB9S connector (J2) located on the SATPAK-PCI bracket. The J2 connector can be used to communicate with a conventional personal computer serial port. This can be useful to execute GPS provider software (TSIPCHAT, LABMON, GPS93) that relies on standard serial port assignments. An additional DB9S connector (J3) will communicate with the second GPS I/O channel that is used to receive RTCM SC-104 differential correction signals and transmit TSIP, TAIP, or NMEA protocol messages. The J2 and J3 bracket connectors utilize RS232 signal levels and are configured as Data Communication Equipment (DCE).

PCI Interface: The SATPAK-PCI utilizes a PLX9050 PCI Bus Target Interface Chip when choosing to communicate with the GPS receiver via the PCI Bus. The PLX9050 incorporates a local bus that is used to interface with a PC16550 UART. The UART converts the serial TTL data required by the GPS receiver to parallel data required by the PLX9050 local bus.

PCI Interrupts: PCI Bus interrupts are selectable from either one of two sources. The first source is the interrupt associated with the UART, and the second interrupt source is the 1PPS signal generated by the GPS receiver.

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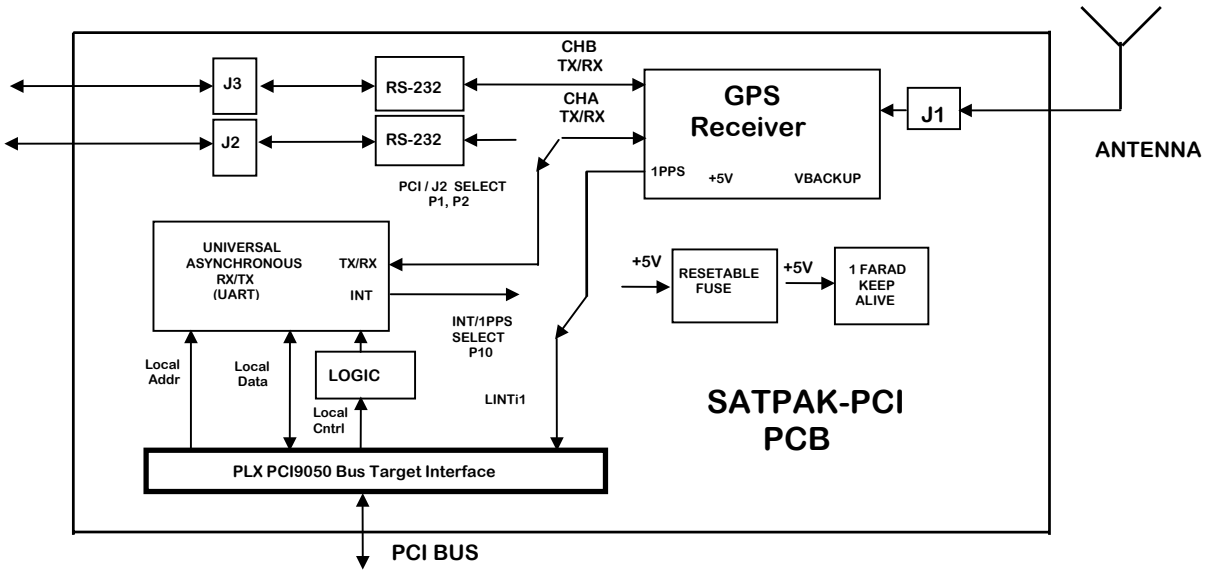
SATPAK-PCI SPECIFICATIONS



Mechanical, Environmental, Power:

Dimensions:	6.6" x 4.2" (167.64mmx106.68 mm)
Operating Temp:	-10°C to 70° C
Extended Temp:	-40°C to +85°C operating
Power:	+5VDC +/- 5%, @265 mA, with GPS and antenna
Fabrication:	Multilayer, 1.68mm ± 0.2mm, FR4

GPS Receiver Keep-Alive:

1 Farad Gold Capacitor used to retain almanac, ephemeris, and real-time clock of GPS receiver for 2-3 weeks after primary power (+5V) is removed.

Connectors:

GPS Antenna Input:	J1
Conn:	Active antenna Input +5VDC output on center lead for antenna power.
Type:	BNC Bulkhead Jack (SMA Optional)
GPS TX/RCV (CHA):	J2 (for PCI bypass mode)
Conn:	Primary GPS TX/RCV
Type:	DB9S Right-Angle PCB mount
Note: J2 only used in PCI bypass mode	
GPS TX/RCV (CHB):	J3
Conn:	Secondary GPS TX/RCV (RTCM)
Type:	DB9S Right-Angle PCB mount

PCI Bus INTA Interrupt Sources (Selectable with P10):

Interrupt Source 1:	INT from 16550 UART
Interrupt Source 2:	1PPS from GPS receiver

PCI Bus Interface:

Addressing Type:	PCI I/O space (8 consecutive bytes)
Interrupt Levels:	INTA
Register Assignments:	Register Assignments are standard PC16550 assignments as follows:

PCI Bus Register Offset Assignments:

The SATPAK-PCI is essentially a COM port on the PCI Bus. In x86 based systems with a PCI Bus, the PCI BIOS will set the SATPAK-PCI configuration registers 1Ch (PCI base address 3 for Local Bus Address Space 1) to a base PCI Bus I/O address in the PCI address space. This value is added to the PC16550 UART offsets to generate PCI Bus addresses. The UART offset registers are shown below. In non x86 environments, the PCI I/O space may be mapped to host processor MEMORY space for machines that don't have I/O instructions.

Offset: From Base	Description	R/W
0	Receive Buff Register	Read
0	Transmit Hold Register	Write
1	Int Enable Register R/W	
2	Int Ident Register	Read
2	FIFO Control Register	Write
3	Line Control Register	R/W
4	Modem Control Register	R/W
5	Line Status Register R/W	
6	Modem Status Register	R/W
7	Scratch Register	R/W

Sample Program. Diagnostics, and WindowsNT v4.0 Driver:

A set of Sample C programs is provided to familiarize the user with interfacing to the SATPAK-PCI via the PCI Bus. A set of diagnostics is also provided that will assist the integrator to verify that the BIOS or OS sees the SATPAK-PCI and display the PCI configuration registers. A WindowsNT v4.0 COM port driver is also provided that will configure the SATPAK-PCI for an unused COM port and IRQ level. After the COM port driver is executed, then GPS communication can be performed using the assigned COM port and IRQ level.

Ordering Information:

Please use the following configuration part identifiers to order your unit with the desired GPS receiver. Add the "SMA" suffix if an SMA connector is desired for J1 instead of the standard BNC.

SATPAK-PCI-T	(Trimble ACEII/ACEIII)
SATPAK-PCI-L	(Trimble SK2/SK8)
SATPAK-PCI-M	(Motorola M12/VP/GT/UT Oncore)
SATPAK-PCI-J	(Navman Jupiter)
SATPAK-PCI-G12	(Ashtech G12 or Thales DG14/DG16)
SATPAK-PCI-C	(Canadian Marconi SuperstarII)